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10/036,955	12/20/2001	Satoru Mayuzumi	NEC 01FN061	4588

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EXAMINER
IM, JUNGHWA M

ART UNIT	PAPER NUMBER
2811	

Norman P. Soloway
HAYES, SOLOWAY, HENNESSEY,
GROSSMAN & HAGE, P.C.
175 Canal Street
Manchester, NH 03101

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/036,955	MAYUZUMI, SATORU	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 21-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 21-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 24-27 recite "...wherein *said visor portion* has *a three-stage* structure comprising a lower part, an upper part with sides, and a visor part with sides, said upper part is isosceles-trapezoidal in shape ... said sides of visor parts and said sides of upper part form an angle of $30\text{-}60^0$."

However, starting on page 10, line 4 (also more explicitly in Figure 5), Applicant's specification recites " The gate electrode 8a as shown in Fig.5 has a three-stage structure consisting of a visor part 8b, an upper part 8c, and a lower part 8d. The visor part 8b is rectangular in section." Therefore, the visor portion can not have a three-stage structure consisting of a visor part, an upper part, and a lower part.

Claims 27-29 are dependent on the rejected base claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 21-23 recite "... wherein said side wall is formed at least two insulation films and every said insulation film contacts *every other* said insulation film." This limitation could be understood that there are at least three insulation films formed for the side wall in order to have one insulating film contacted every other insulting film. However, Figures of the Application explicitly shows that the side wall 9 is formed of only two insulating layers 2, 3. Therefore, examiner assumes that this limitation merely means that two insulating films are in contact with each other.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6, 7, 9, 11, 13, 14, 16, 21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Iguchi et al. (U.S. Pat. No. 5,734,185), hereafter Iguchi.

Regarding claims 1 and 21, Figure 1(a) of Iguchi shows a semiconductor device comprising: a semiconductor substrate 1, a gate insulating film 17, a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion, a side

wall 16 formed on a side the gate electrode, so as to be covered behind a visor of the gate electrode; and an interlayer insulation film 33 in Fig.6(p) covering the gate electrode 20 and being in contact with said side wall, and wherein the sidewall 16 is formed of at least two insulating films 15, 3 and both of the insulating films contacts both the interlayer insulating film and the gate electrode and the insulation films contact each other.

In addition, an interlayer insulation film covering the gate electrode and contacting the side wall would have been inherent as shown by an insulator 33 in Fig.6(p), in order to support upper layers including a gate contact electrode 20, which is necessary for a functioning device.

Regarding claims 3 and 23, Figure 1(a) of Iguchi shows a semiconductor device comprising; a semiconductor substrate 1, a gate insulating film 17 on said semiconductor substrate, a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion, and a side wall 16 formed on a side surface of the gate electrode so as to be covered behind a visor of the gate electrode, said side wall 16 (15, 3) being formed of a lamination of at least two different insulation films having different etching properties (col. 13, lines 24-25), each of the insulating films 15, 3 contacts both the interlayer insulating film and the gate electrode 19 and the insulation films contact each other.

Regarding claims 4 and 6, Figure 1(a) of Iguchi et al. show the gate electrode 19 comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Regarding claims 7 and 9, Figure 1(a) of Iguchi et al. show the width of the visor portion is substantially constant and greater in length along the gate length direction than the upper or lower parts.

Regarding claims 11 and 13, Figure 1(a) of Iguchi shows the side wall is formed on both a side surface of the upper part and a side surface of the lower part.

Regarding claims 14 and 16, Figure 1(a) of Iguchi shows a side surface of the upper parts forms a tapered slope.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5, 8, 10, 12, 15 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi as applied to claims 1, 3, 4, 6, 7, 9, 11, 13, 14 and 16 in view of Kim (U.S. Pat. No. 6,204,538)

Regarding claims 2, 10 and 22, Figure 1(a) of Iguchi shows a semiconductor device comprising: a semiconductor substrate 1, a gate insulating film 17 formed on said semiconductor substrate, a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion, a side wall 16 formed on a side surface of the gate electrode so as to be covered behind a visor of the gate electrode, an interlayer

insulation film 33 in Fig.6(q) covering the gate electrode 20; and a contact 34 formed in interlayer insulation film 33 in Fig.6(q), wherein the sidewall 16 is formed of at least two insulating films 15, 3 and each of the insulating films contacts both the interlayer insulating film and the gate electrode, and the insulation films contact each other.

Iguchi discloses a substantially identical device recited in pending claim except limitation over the contact in a diffused layer on the substrate.

However, Fig. 4C of Kim shows contact 60b extending from gate electrode 30b1 to drain region 40b, and the contacting the vertical side wall of the gate electrode.

It would have been obvious to include a similar contact in the device of Iguchi in order to implement an SRAM cell having this particular circuit connection of gate shorted to drain as discussed at col.4, lines 28-37 of the specification of Kim.

Regarding the limitations for the claims 5, 8, 12 and 15 are discussed above in claims 4, 7, 11 and 14 respectively with 35 USC § 102 rejection.

Claims 24, 26, 27, 29, 30, 32, 33, 35, 36, 38, 39 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi in view of Satoh et al. (U.S. Pat. No. 5,834,817), hereafter Satoh.

Regarding claim 24, insofar as understood, Figure 1(a) of Iguchi shows a semiconductor device comprising: a semiconductor substrate 1; a gate insulating film 17; a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; a side wall 16 formed on a side the gate electrode, so as to be covered behind a visor of the gate electrode; and an interlayer insulation film 33 in Fig.6(p)

covering the gate electrode 20 and being in contact with said side wall and the gate electrode having an upper portion of substantially a trapezoidal shape and a lower portion; and the upper portion connecting the visor portion and the lower portion.

In addition, an interlayer insulation film covering the gate electrode and contacting the side wall would have been inherent as shown by an insulator 33 in Fig.6(p), in order to support upper layers including a gate contact electrode 20, which is necessary for a functioning device.

Figure 1(a) of Iguchi shows substantially the entire claimed structure except "said sides of visor part and said sides of upper part form an angle of 30^0-60^0." Fig. 4D of Satoh shows a gate structure with the sides of the visor part and the sides of the upper part forming an angle on the order of about 30^0. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the angle of the upper portion of the Iguchi's gate with the teaching of Satoh in order to accommodate an obvious design variation of the gate shape.

Also note that it would have been obvious to one of ordinary skill in the art at the time of the invention to have an intended range of the tapered angle for the upper portion of the gate electrode recited in pending claim, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 26, insofar as understood, Figure 1(a) of Iguchi shows a semiconductor device comprising; a semiconductor substrate 1; a gate insulating film 17 on said semiconductor substrate; a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said

gate electrode further having a visor portion; and a side wall 16 formed on a side surface of the gate electrode so as to be covered behind a visor of the gate electrode, said side wall 16 (15, 3) being formed of a lamination of at least two different insulation films having different etching properties (col. 13, lines 24-25), and the gate electrode having an upper portion of substantially a trapezoidal shape, and a lower portion; and the upper portion connecting the visor portion and the lower portion.

Regarding claims 27 and 29, Figure 1(a) of Iguchi shows said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Regarding claim 30, Figure 1(a) of Iguchi shows a semiconductor device comprising: a semiconductor substrate 1, a gate insulating film 17, a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion, a side wall 16 formed on a side the gate electrode, so as to be covered behind a visor of the gate electrode; and an interlayer insulation film 33 in Fig.6(p) covering the gate electrode 20 and being in contact with said side wall.

In addition, an interlayer insulation film covering the gate electrode and contacting the side wall would have been inherent as shown by an insulator 33 in Fig.6(p), in order to support upper layers including a gate contact electrode 20, which is necessary for a functioning device.

Iguchi shows substantially the entire claimed structure except the visor portion without overhang. Fig. 4D of Satoh shows a gate structure which is identical to the pending claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the shape of the Iguchi's gate with the teaching of Satoh in

order to accommodate an obvious design variation of the gate shape as shown Figures 4C-4F of Satoh.

Regarding claim 32, Figure 1(a) of Iguchi shows a semiconductor device comprising; a semiconductor substrate 1, a gate insulating film 17 on said semiconductor substrate, a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion, and a side wall 16 formed on a side surface of the gate electrode so as to be covered behind a visor of the gate electrode, said side wall 16 (15, 3) being formed of a lamination of at least two different insulation films having different etching properties (col. 13, lines 24-25), each of the insulating films 15, 3 contacts both the interlayer insulating film and the gate electrode 19 and the insulation films contact each other.

Iguchi shows substantially the entire claimed structure except the visor portion without overhang. Fig. 4D of Satoh shows a gate structure which is identical to the pending claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the shape of the Iguchi's gate with the teaching of Satoh in order to accommodate an obvious design variation of the gate shape as shown Figures 4C-4F of Satoh. Therefore, it would be also obvious that the sidewalls of the modified Iguchi's gate structure would be formed only below the visor portion to utilize the self-alignment process of the side wall formation.

Regarding claims 33 and 35, Figure 1(a) of Iguchi et al. show the gate electrode 19 comprises a lower part substantially constant in the length along said gate length

direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Regarding claims 36 and 38, Figure 1(a) of Iguchi shows the side wall is formed on both a side surface of the upper part and a side surface of the lower part. It would be also obvious that the sidewalls of the modified Iguchi's gate structure would be formed only below the visor portion to utilize the self-alignment process of the side wall formation.

Regarding claims 39 and 41, Figure 1(a) of Iguchi shows a side surface of the upper parts forms a tapered slope.

Claims 25, 28, 31, 34, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi and Kim as applied to claim 2 above, and further in view of Satoh.

Regarding claim 25, Figure 1(a) of Iguchi shows a semiconductor device comprising: a semiconductor substrate 1; a gate insulating film 17 formed on said semiconductor substrate; a gate electrode 19 formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; a side wall 16 formed on a side surface of the gate electrode so as to be covered behind a visor of the gate electrode; an interlayer insulation film 33 in Fig.6(q) covering the gate electrode 20; and a contact 34 formed in interlayer insulation film 33 in Fig.6(q).

Iguchi discloses most aspect of the pending claim except limitation over the contact in a diffused layer on the substrate and the sides of visor part and the sides of upper part forming an angle of 30^0-60^0.

However, Fig. 4C of Kim shows contact 60b extending from gate electrode 30b1 to drain region 40b, and the contacting the vertical side wall of the gate electrode.

It would have been obvious to include a similar contact in the device of Iguchi in order to implement an SRAM cell having this particular circuit connection of gate shorted to drain as discussed at col.4, lines 28-37 of the specification of Kim.

The combined teachings of Iguchi and Kim disclose the substantially the entire claimed structure except the sides of visor part and the sides of upper part forming an angle of 30^0-60^0. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the angle of the upper portion of the gate of Iguchi and Kim with the teaching of Satoh in order to accommodate an obvious design variation of the gate shape.

Also note that it would have been obvious to one of ordinary skill in the art at the time of the invention to have an intended range of the tapered angle for the upper portion of the gate electrode recited in pending claim, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 28, Figure 1(a) of Iguchi shows said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Regarding claim 31, the combined teaching of Iguchi and Kim show substantially the entire claimed structure except the visor portion without overhang. Fig. 4D of Satoh

shows a gate structure which is identical to the pending claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the shape of the Iguchi's gate with the teaching of Satoh in order to accommodate an obvious design variation of the gate shape as shown Figures 4C-4F of Satoh. Therefore, it would be also obvious that the sidewalls of the modified Iguchi's gate structure would be formed only below the visor portion to utilize the self-alignment process of the side wall formation.

Regarding claim 34, Figure 1(a) of Iguchi et al. show the gate electrode 19 comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Regarding claim 37, Figure 1(a) of Iguchi shows the side wall is formed on both a side surface of the upper part and a side surface of the lower part. It would be also obvious that the sidewalls of the modified Iguchi's gate structure would be formed only below the visor portion to utilize the self-alignment process of the side wall formation.

Regarding claim 40, Figure 1(a) of Iguchi shows a side surface of the upper parts forms a tapered slope.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection. The rejection stands, modified only

to accommodate the amendments made the Claims by applicant. New rejections are made in response to Applicant's amended claims.

Examiner sincerely apologize a typological error regarding claim 23 in paper No. 11. However, claim 23 was rejected along with claim 3 with the reference of Iguchi, clearly meeting all the limitations recited in the claim.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
November 3, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800